PC

TGLDx
Thin Glenn-Lund w/Discriminators for InterpolatingPad Chambers

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PC *detector specifications*

	PC1	PC2	PC3
• detector capacitance:	5pF	16pF	20pF
• charge sensitivity / MIP:	18fC	29fC	36fC
• min. charge of interest:	0.9fC	1.45fC	1.8fC
• max channel rate:	200 counts / second		

PC *tgld function*

- charge sensitive preamp with programmable reset, decay & channel disable
- passive CR differentiation
- leading edge discriminator with programmable threshold
- On chip charge calibration
- 16 channels per chip
- 1 milliwatt per channel

PC tgld preamp specifications

	pc1	pc2	pc3
charge gain to input of differentiator(mV / fC):	20	12.4	10
MIP gain (mV / MIP)	360	360	360
maximum linear / rail output voltage:	1.3 / 1.6 V		
maximum linear charge (fC):	65	105	130
maximum linear in MIPs:	3.6	3.6	3.6
rail output in MIPs:	> 7	> 7	> 7
signal / noise:	> 4:1 @ < 20pF		
bias equalized risetime(nsec):	100	100	100
programmable decay time:	500nsec - 32µsec.		

- feedback shorting reset switches
- onboard charge calibrator: 1-16fC(1fC steps), 10-160(10fC steps)
- nominal 100 nsec. **CR** passive output differentiator
- 200 µW per channel
- 16 channels per chip

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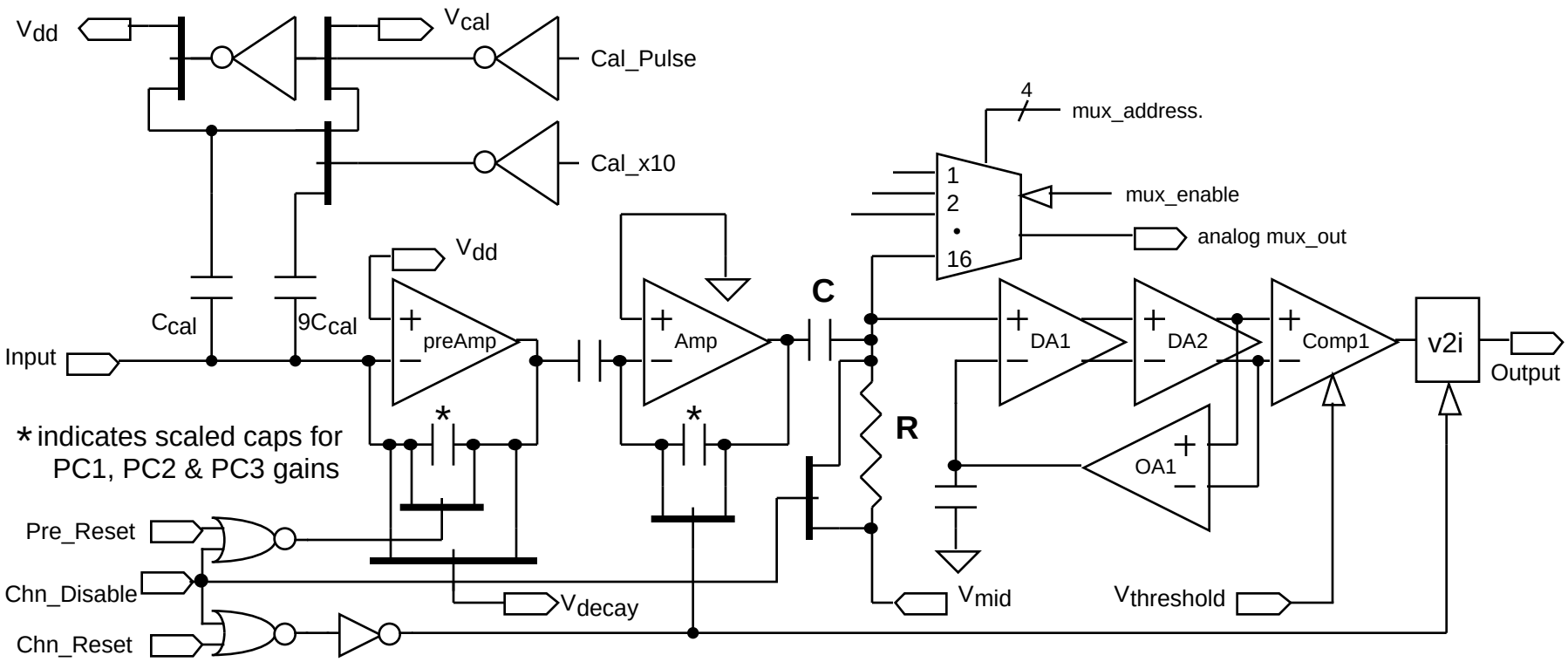
tgld typical channel



PC *tgld discriminator specifications*

- leading edge discriminator
- programmable threshold: 10 - 320 mV (6-bit DAC)
- maximum input offset: ±5mV
- maximum delay time: 70 nsec
- maximum reset time: 150 nsec (actual reset time is dependent on input tail)
- current output(nominal): 100 µA asserted, 0 µA un asserted
- 800µW per channel
- programmable channel disable
- 16 channels per chip

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PC manufacturing plan

- Orbit or H-P 1.2 µm CMOS process with linear caps
- design new tgld after major requirements revision 9/96 (Dec 96)
- protype thru Orbit Foresight or MOSIS brokerage and test revised design (parts out Mar 97)
- tweak new design based on evaluation units (Apr 97)
- fab short lot of preproduction wafers and test for “known good die” with MOSIS’ IMS tester and special ORNL supplied test boards and vectors (Jul 97)
- develop Iqq test vectors and reject/accept criteria (Aug 97)
- fab production wafer run thru Orbit or H-P and wafer test with Iqq requirements (Nov 97)

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PC preamp/disc. test plans

- Acquire dedicated probe card for tgldx to fit MOSIS test station
- develop any special hardware to test analog portions in conjunction with IMS digital tester at MOSIS
- evaluate 1st silicon of revised tgldx at die level at MOSIS and on ROC at Lund
- attempt Iqq testing on short wafer run of tgldx at MOSIS
- determine if Iqq testing is feasible for analog screening for Known Good Die
- develop special HW & SW for production testing of ROC
- test production run of tgldx at MOSIS with Iqq or special HW

PC development status

- TGLDx chips
  - three designs; one each for PC1, PC2 & PC3
  - design complete in Dec 1996
  - Prototype run for TGLD1, TGLD2 & TGLD3 in Dec 1996
  - single fab run with shared retical
  -
- readout card
  - layout new ROC based on TGLDx pinout Nov 1996